

IN THE CLAIMS:

Please CANCEL claims 30, 32, 36 and 40 without prejudice or disclaimer of the subject matter recited therein.

Please AMEND the claims to read as follows:

28. (Amended) A semiconductor device, comprising:  
a substrate;  
a gate electrode provided on said substrate;  
a diffusion region formed in said substrate adjacent to said gate electrode;  
a side-wall insulation film formed on a side wall of said gate electrode;  
a self-aligned contact hole defined by said side-wall oxide film and exposing said diffusion region; and  
a silicide region formed selectively on a surface of said diffusion region;  
wherein said semiconductor device further includes;  
a first insulation film provided on said gate electrode so as to cover said side wall oxide film partially;  
a second insulation film having a composition different from a composition of said first insulation film and provided on said first insulation film;  
an interlayer insulation film deposited on said second insulation film;

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*am*

a contact hole formed in said interlayer insulation film, said contact hole extending through said first and second insulation films and exposing said self-aligned contact hole;  
said first insulation film contacts H<sub>2</sub>O with an amount smaller than about 2.4 wt%.

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31. (Amended) A semiconductor device as claimed in claim 28, further comprising a conductor pattern contacting with said diffusion region and said gate electrode such that said conductor pattern extends along a surface of said side wall oxide film.

33. (Amended) A semiconductor device as claimed in claim 28, further comprising another silicide region formed selectively on a surface of said gate electrode.

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34. (Amended) A semiconductor device, comprising:

a substrate;

a gate electrode provided on said substrate;

a diffusion region formed in said substrate adjacent to said gate electrode;

a side-wall insulation film formed on side wall of said gate electrode;

a self-aligned contact hole defined by said side-wall oxide film and exposing said diffusion region; and

a silicide region formed selectively on a surface of said diffusion region, wherein said semiconductor device further includes:

a first insulation film provided on said gate electrode so as to cover said side wall oxide film partially;

a second insulation film having a composition different from a composition of said first insulation film and provided on said first insulation film;

an interlayer insulation film deposited on said second insulation film;

a contact hole formed in said interlayer insulation film, said contact hole extending through said first and second insulation films and exposing said self-aligned contact hole;

said first insulation film is formed of PSG containing P with an amount of about 6 wt% or less.

35. (Amended) A semiconductor device as claimed in claim 34, further comprising a conductor pattern contacting with said diffusion region and said gate electrode such that said conductor pattern extends along a surface of said side wall oxide film.

37. (Amended) A semiconductor device as claimed in claim 34, further comprising another silicide region formed selectively on a surface of said gate electrode.

38. (Amended) A semiconductor device, comprising:  
a substrate;  
a gate electrode provided on said substrate;

a diffusion region formed in said substrate adjacent to said gate electrode;  
a side-wall insulation film formed on a side wall of said gate electrode;  
a self-aligned contact hole defined by said side-wall oxide film and exposing said diffusion region; and

a silicide region formed selectively on a surface of said diffusion region,  
wherein said semiconductor device further includes:  
a first insulation film provided on said gate electrode so as to cover said side wall oxide film partially;

a second insulation film having a composition different from a composition of said first insulation film and provided on said first insulation film;

an interlayer insulation film deposited on said second insulation film;  
a contact hole formed in said interlayer insulation film, said contact hole extending through said first and second insulation films and exposing said self-aligned contact hole;

said first insulation film is formed of BPSG containing B with an amount of about 4 wt% or less.

39. (Amended) A semiconductor device as claimed in claim 38, further comprising a conductor pattern contacting with said diffusion region and said gate electrode such that said conductor pattern extends along a surface of said side wall oxide film.

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41. (Amended) A semiconductor device as claimed in claim 38, further comprising another silicide region formed selectively on a surface of said electrode.

Please ADD new claim 42 as follows:

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42. A method of fabricating a semiconductor device, comprising the steps of:  
(A) forming a refractory metal layer on a diffusion region in a semiconductor substrate;  
(B) forming a self-aligned silicide layer on said refractory metal layer by applying a heat-treatment process;  
(C) forming an insulation film on a surface of said silicide layer by conducting a plasma CVD process while using a source gas containing SiH<sub>4</sub> and N<sub>2</sub>O with a ratio of N<sub>2</sub>O with respect to SiH<sub>4</sub> equal to or less than 5;  
(D) forming a nitride film, after said step (C), on said insulation film in contact with said insulation film, without exposing a surface of said insulation film to the air;  
(E) forming an interlayer insulation film so as to cover said nitride film; and  
(F) forming a window exposing said silicide layer, by applying a dry etching process consecutively to said interlayer insulation film, said nitride film, and said insulation film.